# Band-pass filter for spectral analyzers
## BA3830S

The BA3830S is a 6 + 1 band band-pass filter for spectral analyzer displays with internal recording indicator output. All of the capacitors comprising the filter are internal capacitors, making it possible to significantly reduce the number of attached components. This enables configuration of compact sets with a high level of reliability.

●Applications

CD radio cassette players, mini-components, car stereos

●Features

1) Six internal band-pass filters for spectral analyzers
2) Internal input/output for recording indicators
3) Internal capacitors reduce the number of attachments.

●Absolute maximum ratings (Ta = 25°C)

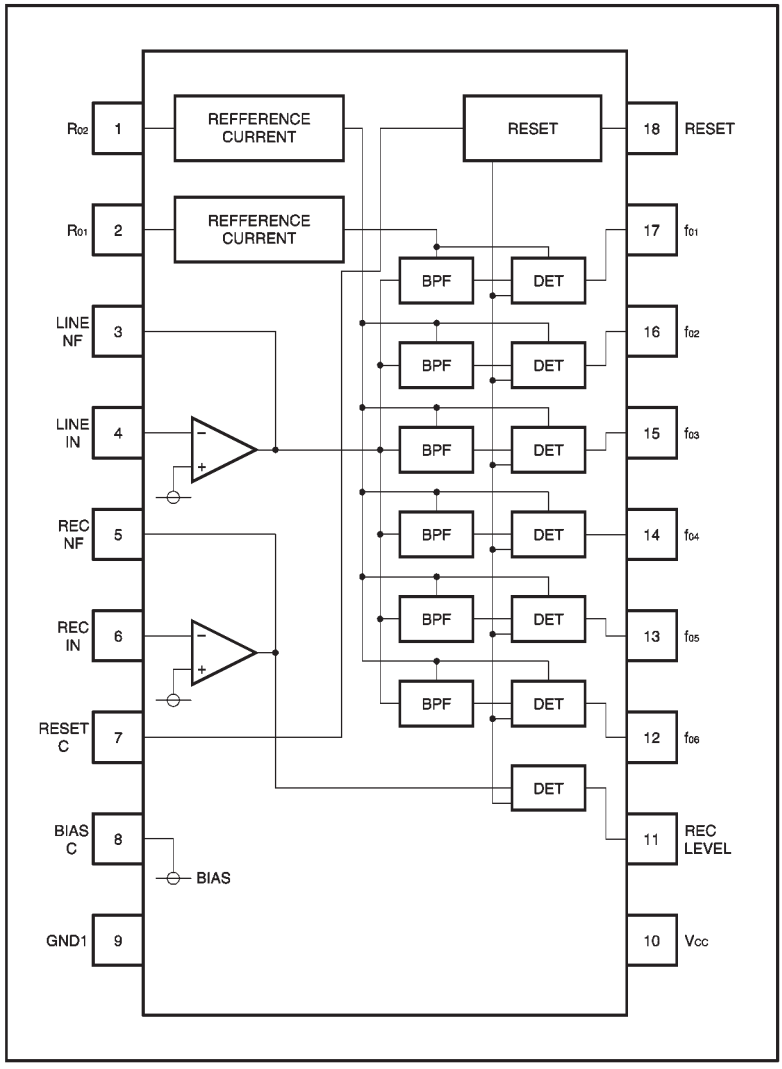
| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 9 | V |
| Power dissipation | Pd | 600* | mW |
| Operating temperature | Topr | −25～+75 | ℃ |
| Storage temperature | Tstg | −55～+150 | ℃ |

* Reduced by 6.0mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Operating power supply voltage | $V_{CC}$ | 4.5 | — | 8.0 | V |

●Block diagram



●Electrical characteristics (unless otherwise noted, Ta = 25°C, $V_{CC}$ = 5V, $R_L$ = 10MΩ, $R\phi_1$ = 270kΩ, $R\phi_2$ = 270kΩ)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Coniditions |
|---|---|---|---|---|---|---|
| Quiescent current | Io | — | 3.8 | 5.2 | mA | |
| Reference output level (LEVEL) | $V_{ol}$ | −3 | 0 | 3 | dB | $V_{IN}$=−30dBV, $V_o$=1.5V (0dB) When f=center frequencies is input |
| Max. output level (LEVEL) | $V_{olmax}$ | 3.2 | 4.2 | — | V | $V_{IN}$=−14dBV, When f=center frequencies is input |
| Reference output level (REC LEVEL) | $V_{or}$ | −3 | 0 | 3 | dB | $V_{IN}$=−30dBV, $V_o$=1.5V (0dB) f=1kHz |
| Max. output level (REC LEVEL) | $V_{olmax}$ | 3.8 | 4.8 | — | V | $V_{IN}$=−14dBV, f=1kHz |
| Output offset voltage | $V_{off}$ | — | 30 | 90 | mV | With no signal |
| Center frequency 1 | $f_{01}$ | 49 | 63 | 77 | Hz | $V_{IN}$=−30dBV |
| Center frequency 2 | $f_{02}$ | 117 | 150 | 183 | Hz | $V_{IN}$=−30dBV |
| Center frequency 3 | $f_{03}$ | 257 | 330 | 403 | Hz | $V_{IN}$=−30dBV |
| Center frequency 4 | $f_{04}$ | 0.78 | 1 | 1.22 | kHz | $V_{IN}$=−30dBV |
| Center frequency 5 | $f_{05}$ | 2.55 | 3.3 | 4.03 | kHz | $V_{IN}$=−30dBV |
| Center frequency 6 | $f_{06}$ | 7.8 | 10 | 12.2 | kHz | $V_{IN}$=−30dBV |
| Input current when Reset pin is HIGH | $I_{IN}$ | 150 | 215 | 280 | μA | $V_{IN}$=5V |
| Threshold level when Reset pin is ON | $V_{th}$ | — | 1.4 | 1.8 | V | |
| Threshold level when Reset pin is OFF | $V_{th}$ | 1.0 | 1.4 | — | V | |

*Q is set to 4.5.
◎Not designed for radiation resistance.

●Measurement circuit

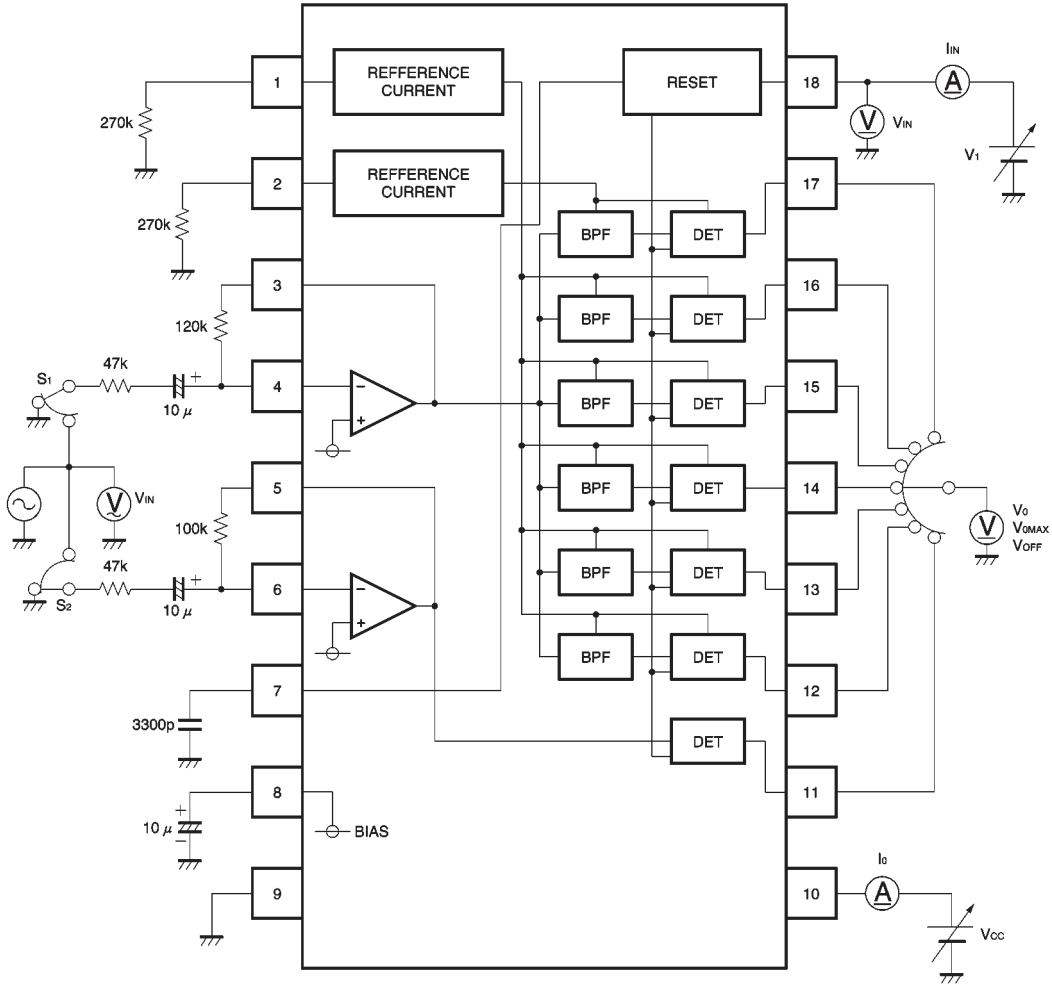
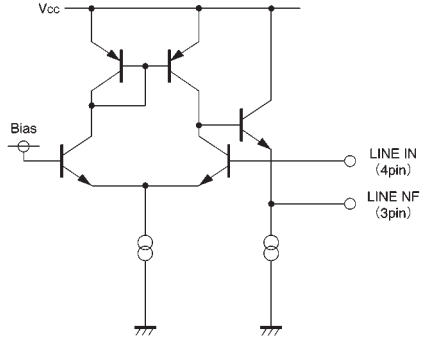



Fig.1

●Circuit operation

(1) LINE and REC input circuits

The LINE and REC input circuits are configured as differential amplifiers, and the gain can be set to any desired value using an external resistor. The input impedance is determined by the external resistor.




(Note: All resistance values in the internal circuit diagrams noted here are reference values.)

Fig.2

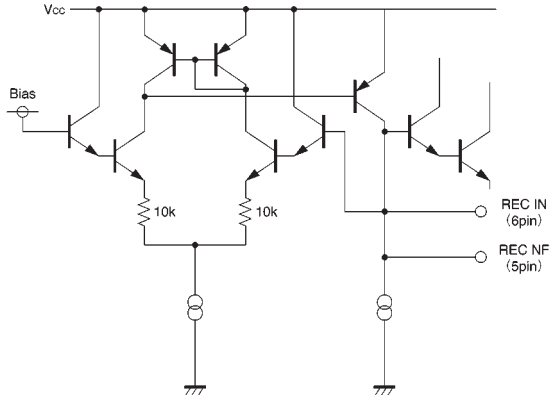
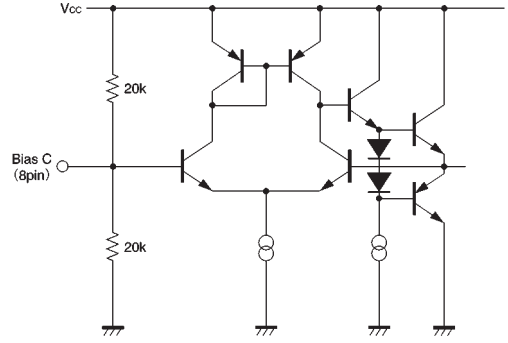



Fig.3

(2) Bias circuit

A bias voltage of $V_{CC}/2$ is applied to each of the circuits. Since the output stage uses a push-pull configuration, a stable bias source can be obtained.




(Note: All resistance values in the internal circuit diagrams noted here are reference values.)

Fig.4

(3) BPF circuit

This is a circuit that selects the required frequency component from the input signal and amplifies it. With this configuration, no external capacitor is needed. In addition, the center frequency is set based on the current, so $f_{01}$ and $f_{02}$ to $f_{06}$ can be set individually, using separate external resistors (pins1 and 2).

Q is set to 4.5V (Typ.).

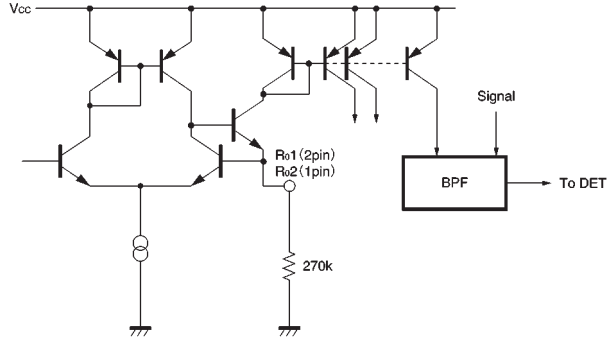



Fig.5

(4) DET circuit

This circuit carries out phase detection on the signal selected and amplified by the BPF, and holds it at the peak level. It is configured so that all of the capacitors are internal.

The charge that was charged by the internal capacitors in the DET circuit is set to be discharged at 75ms/V (Typ.), but in order to eliminate any effects of disparity, a reset circuit is also included.

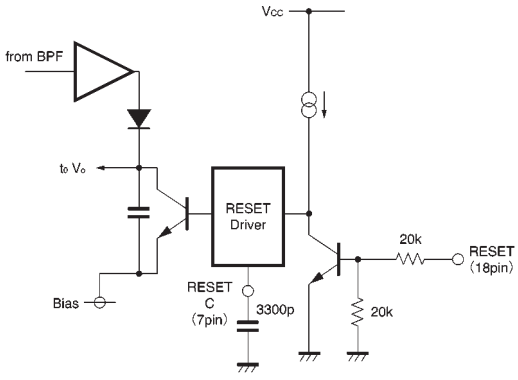



Fig.6

(5) Output section circuit

The signal level held at peak level by the DET undergoes V/I conversion and is output. Since the next stage supports MOS (high-input impedance), there is a resistance of 33.9kΩ (44.3kΩ for REC output only) between the output pin and the GND in the IC, so the output value changes based on the input impedance.

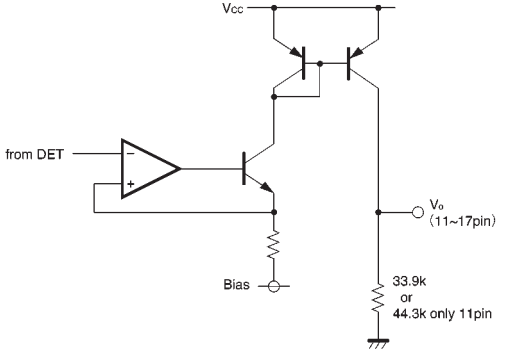



Fig.7

●Application example

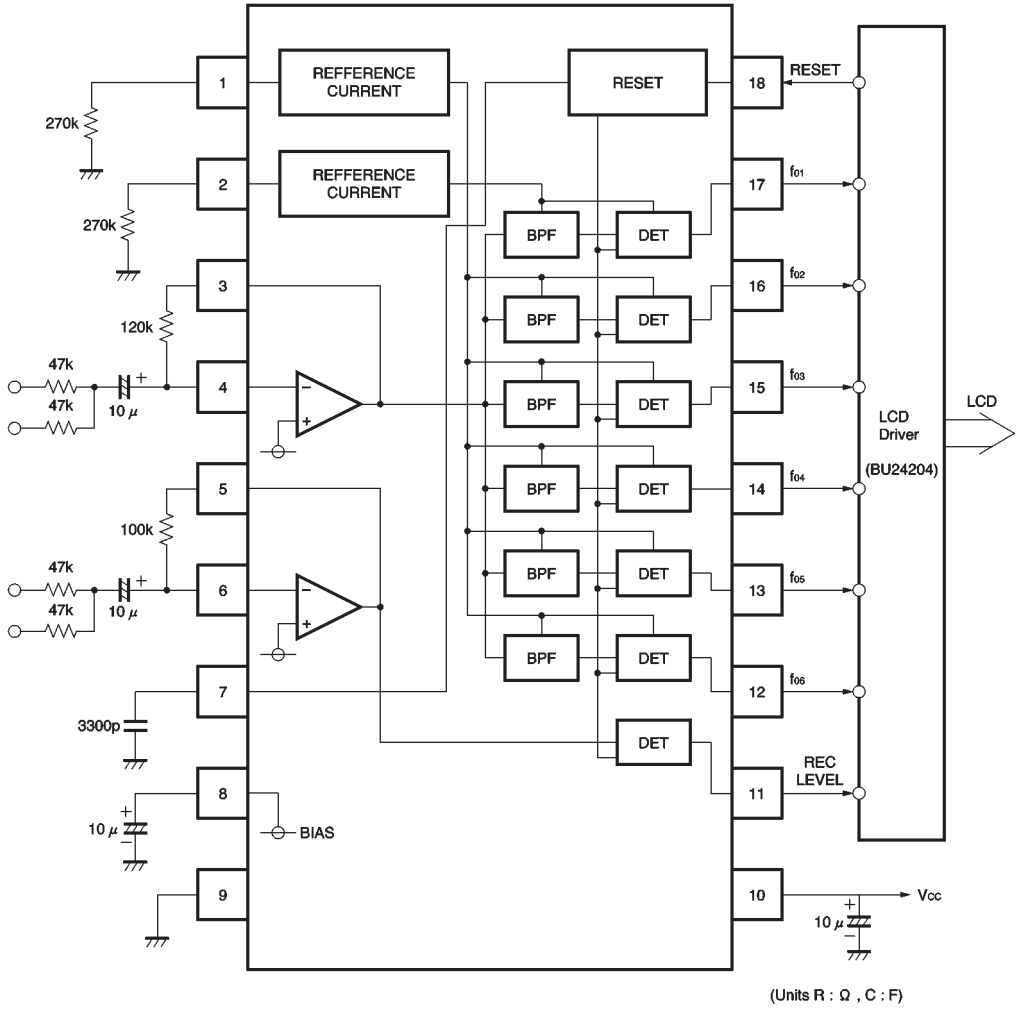



Fig.8

●Operation notes

(1) Precautions concerning the load resistance

The various characteristics were measured at the output resistance value of 10MΩ noted in the specifications manual. Moreover, because the output of this IC supports the MOS configuration, be aware that it is current output, and the output changes depending on the input impedance at the next stage.

(2) Precautions concerning the RESET capacitor

If the reset function is to be used, a capacitor of at least 3300pF is required for RESET C (pin 7). Failing to connect this capacitor can result in erroneous displays, so make sure a sufficient capacitance is provided.

(3) Precautions concerning the coupling capacitor

When determining the polarity of the input electrolytic coupling capacitor, the potential relation with the other end of the coupling must be taken into consideration.

●Electrical characteristic curves

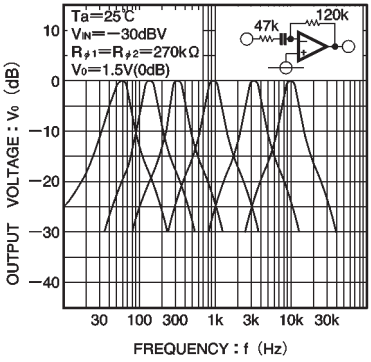



Fig.9 Output vs. frequency

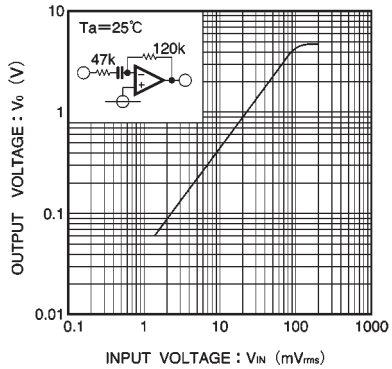



Fig.10 Input vs. output level
($f_{01}$ to $f_{06}$ modes)

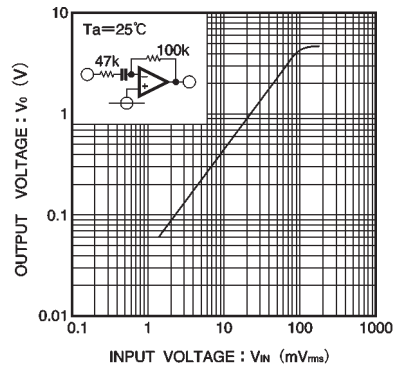
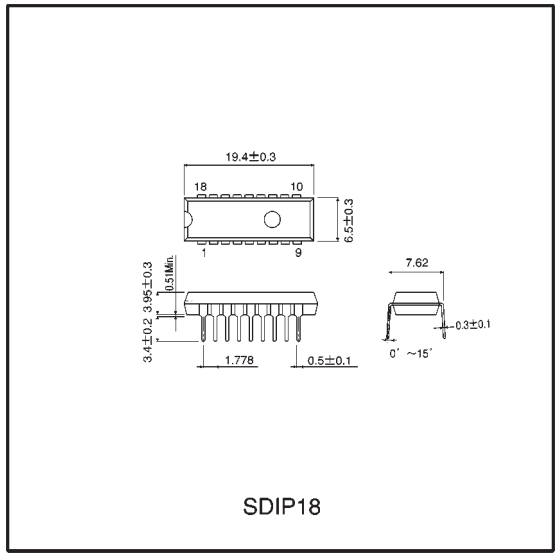



Fig.11 Input vs. output level
(REC mode)

●External dimensions (Units: mm)

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